**THE NATIONAL INSTITUTE OF ENGINEERING**

**(An Autonomous Institute under Visvesvaraya Technological University, Belagavi )**



#### A Report on

#### Course Project - CMOS Level Shifters

#### VLSI LAYOUT DESIGN:EC7L04

##### By

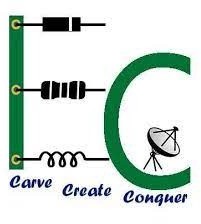
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### ABSTRACT

Level Shifter (LS) circuits are widely used as interfaces for multiple voltage do- mains in moderns ICs and System on Chips (SoCs). Low power dissipation and low delay are the main design considerations for high performance level shifters. This pa- per presents the design of a level shifter integrating new topological modifications to assure a wide range of voltage conversion with low power dissipation and low output delay.A level shifter (LS) translates logic levels between two voltage domains for ex- ample 0, VDD to VL, VH; but in most of cases the designers refer to level shifters as circuits translating at high speed and without static power consumption from 0, VDD to 0, VH ¿ VDD Level shifters can be useful in applications like communicating a low VDD CPU to a 5 V peripheral, in HV displays, nonvolatile memories, driving the gate of a high-side pass transistor in a switched converter, or in medical devices to implement tissue-stimuli delivery subsystems. This family of circuits have a special interest in the case of implantable medical devices where is common to handle previously unknown voltages either positive or negative, above or below the control logic supply VDD.

*Keywords*: Level shifter HV-CMOS Biomedical circuits,CMOS, Delay, Level Shifter, Multi-supply voltage design, SoC, Ultra-Low Power

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## Introduction

In the era of Complementary metal-oxide-semiconductor (CMOS) technology, low power consumption is one of the most key concerns to address in today’s SoCs designs. The demand for low power and low output delay is very high, especially for handheld de- vices like cell phone, tablet etc. CMOS technology is being widely used to meet the increasing demand for low power consumption and low delay operation in microelec- tronics circuit systems. Considerable reduction in chip size (¡1 mm ) has become pos- sible with the advancement of CMOS technology which minimizes the manufacturing cost greatly. In multi-voltage systems, level shifter is a significant circuit component and usually used in between core circuit and input/output (I/O) circuit. Level Shifters are used to convert the voltage level of an input signal to another voltage level at the output node. But the conventional level shifter dissipates high power and suffers from longer delay variation. Hence, the low power dissipation and low operation delay in level shifter have become major design issues for microelectronics circuits. Increases in power dissipation cause rise in reliability issues and limit the device portability.

To meet the increasing demand for low power and high performance ICs, CMOS technology is being aggressively scaled . The most effective way to minimize power dissipation in VLSI and other electronic circuit is to minimize their corresponding sup- ply voltages. This is because of the quadratic dependence of the power dissipation on the supply voltage . The delay variation occurs due to different current driving capa- bilities of transistors . The level shifters are required to function appropriately when the difference between the two voltage levels is high. The high voltage difference may cause the failure of functionality in conventional LS circuit topologies due to low drive current when the supply voltage is very low.

For the purpose of getting lower voltage from the high voltage domain, implement- ing CMOS inverters are normally adequate . But to get higher voltage from a low voltage supply domain in LS circuits, complicated circuit architectures are required. In order to design a simple LS circuit, proper design techniques must be utilized to balance the units of the circuit functioning at the high power supply voltage (VDDH) level with the input unit driving capability of the Level shifter .

## Circuit Working

The schematic of a conventional basic Level shifter is presented in figure 1. The circuit is operated by equivalent input signals IN and INB. It is composed of cross-coupled two NMOS driver transistors (MN1, MN2) and PMOS latch (MP1, MP2). The functionality of the circuit fails when there is a large difference between the high supply voltage VDDH and low supply voltage VDDL. When the voltage IN and INB are low, the MN1 and MN2 go off and MN1 and MN2 turn on when the IN and INB are high, respectively. MP1 will turn ON when the MN2 pulls down the node OUT. Then MP2 goes OFF and OUT will drop down to the GROUND level because the node OUTB increases to VDDH. Furthermore, the voltage of OUT is derived by both pulldown transistor MN2 and drive current of pull-up transistors MP2. Therefore, OUT can’t be discharged if the drive current of MP2 is higher compared to MN2. On the other hand, the OUT can’t be discharged when IN is high and INB is low, and the transistors MN1 and MN2 are

turned ON and OFF respectively.

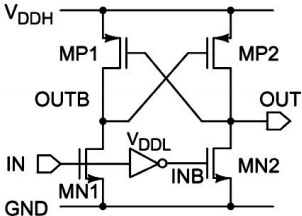


Figure 1: Level Shifter Circuit

## Schematics and Symbol

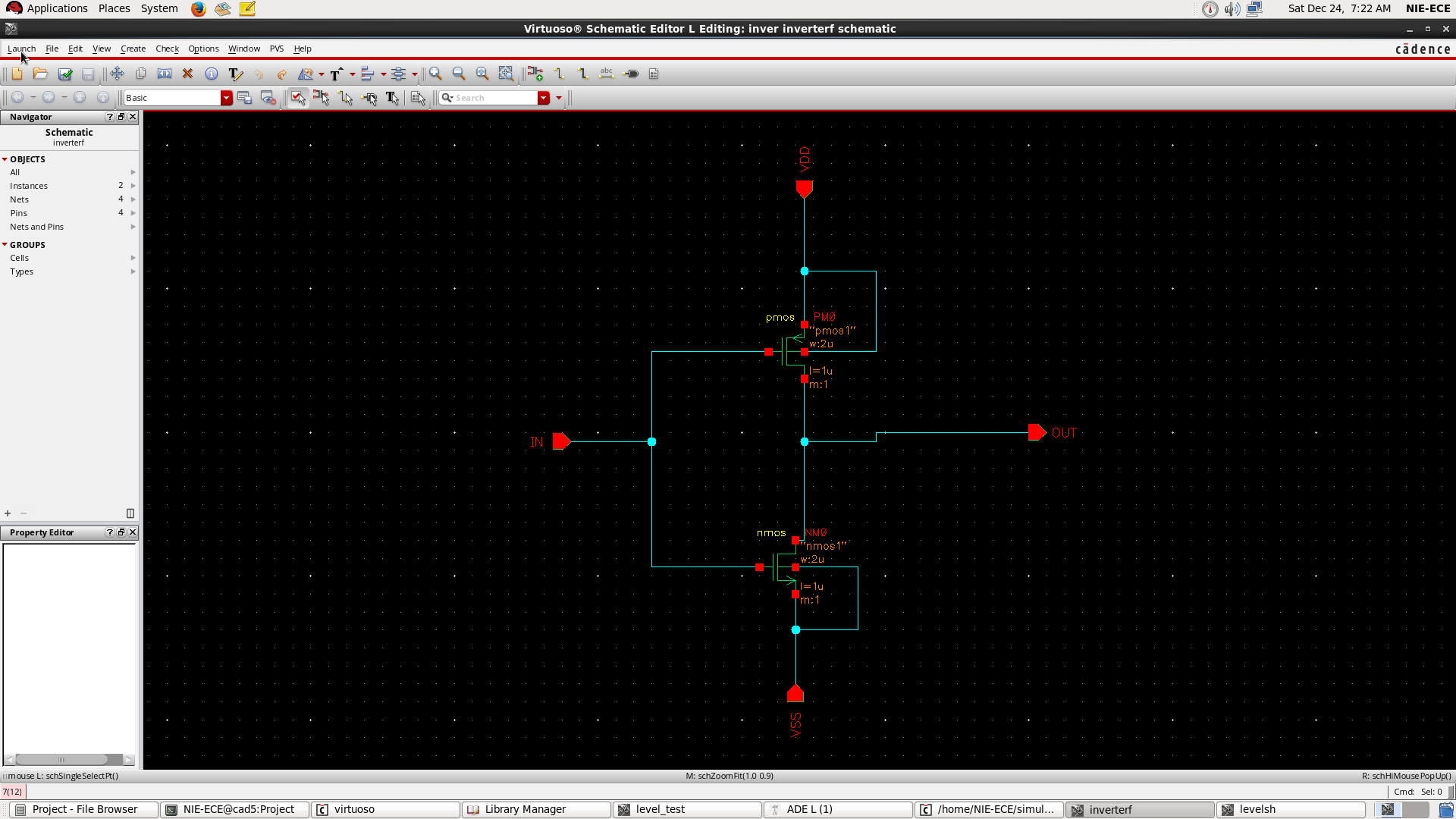


Figure 2: Inverter Schematic

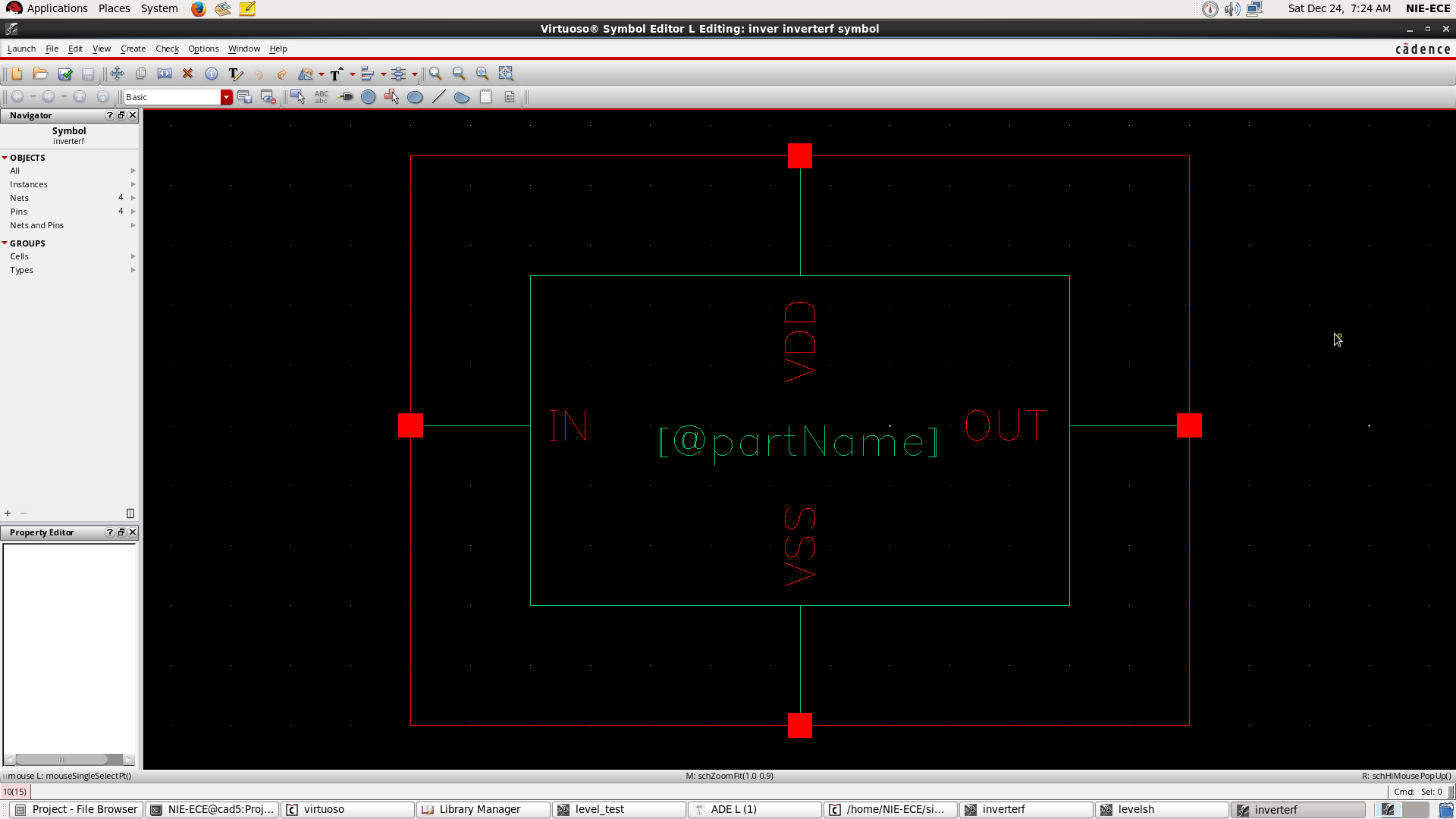


Figure 3: Inverter Symbol

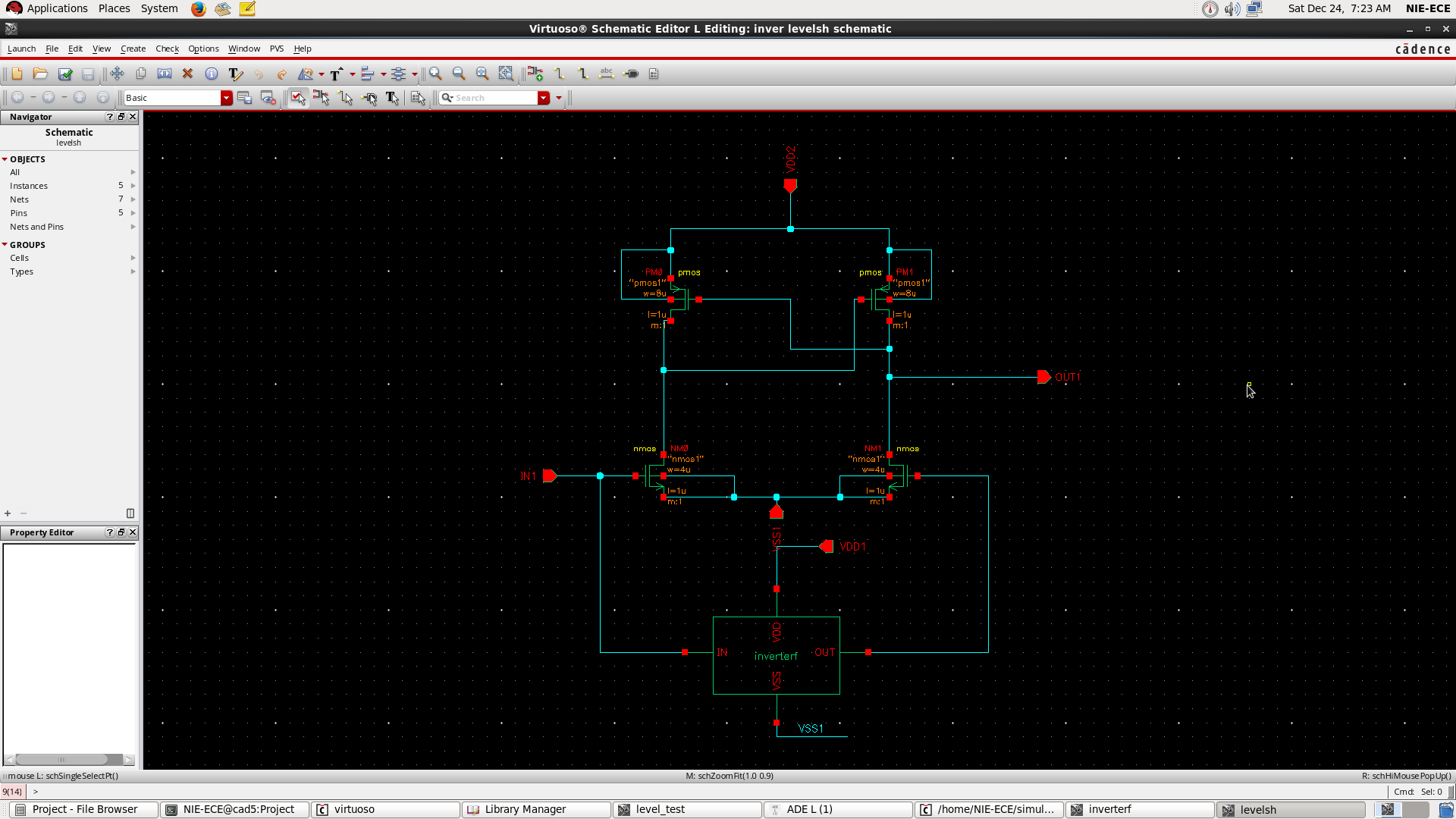


Figure 4: Level Shifter Schematic

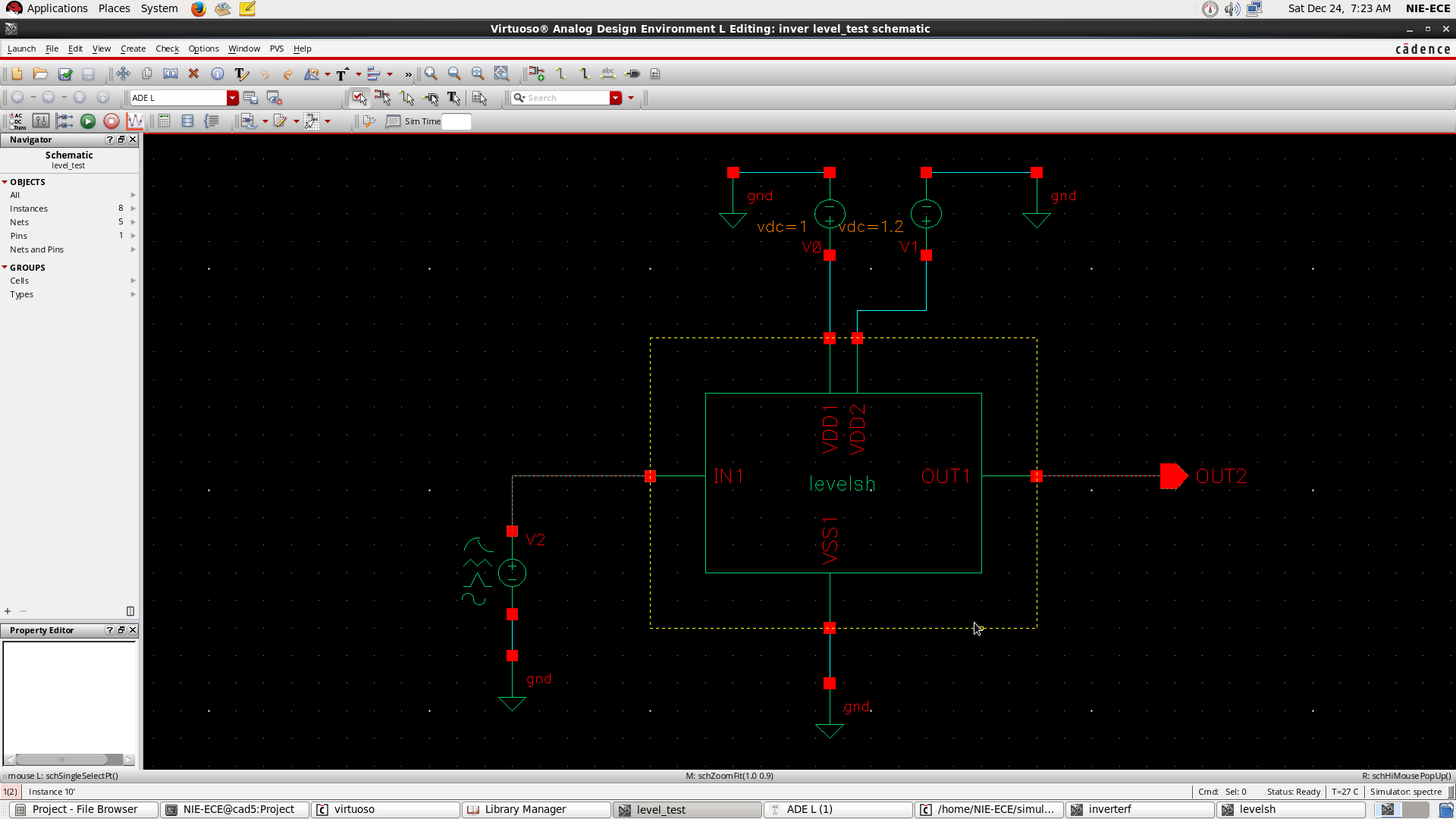


Figure 5: Level Shifter Symbol

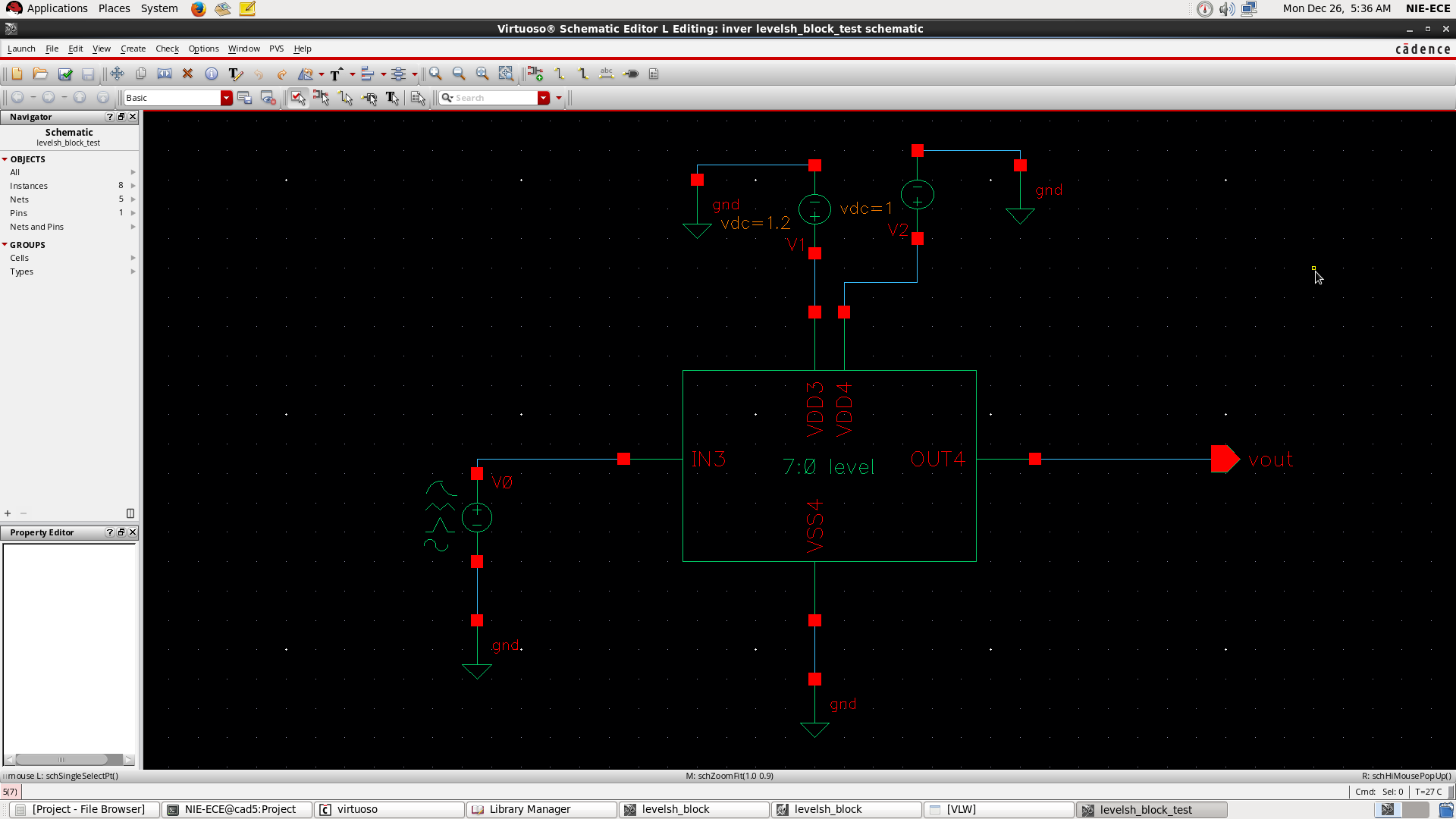


Figure 6: 8-bit Level Shifter

## Layout Design

Layout design is been done in Cadence with the given constraints.

-Top Metal is METAL3.

-Input pins to be placed at South and output pins to be placed at North.

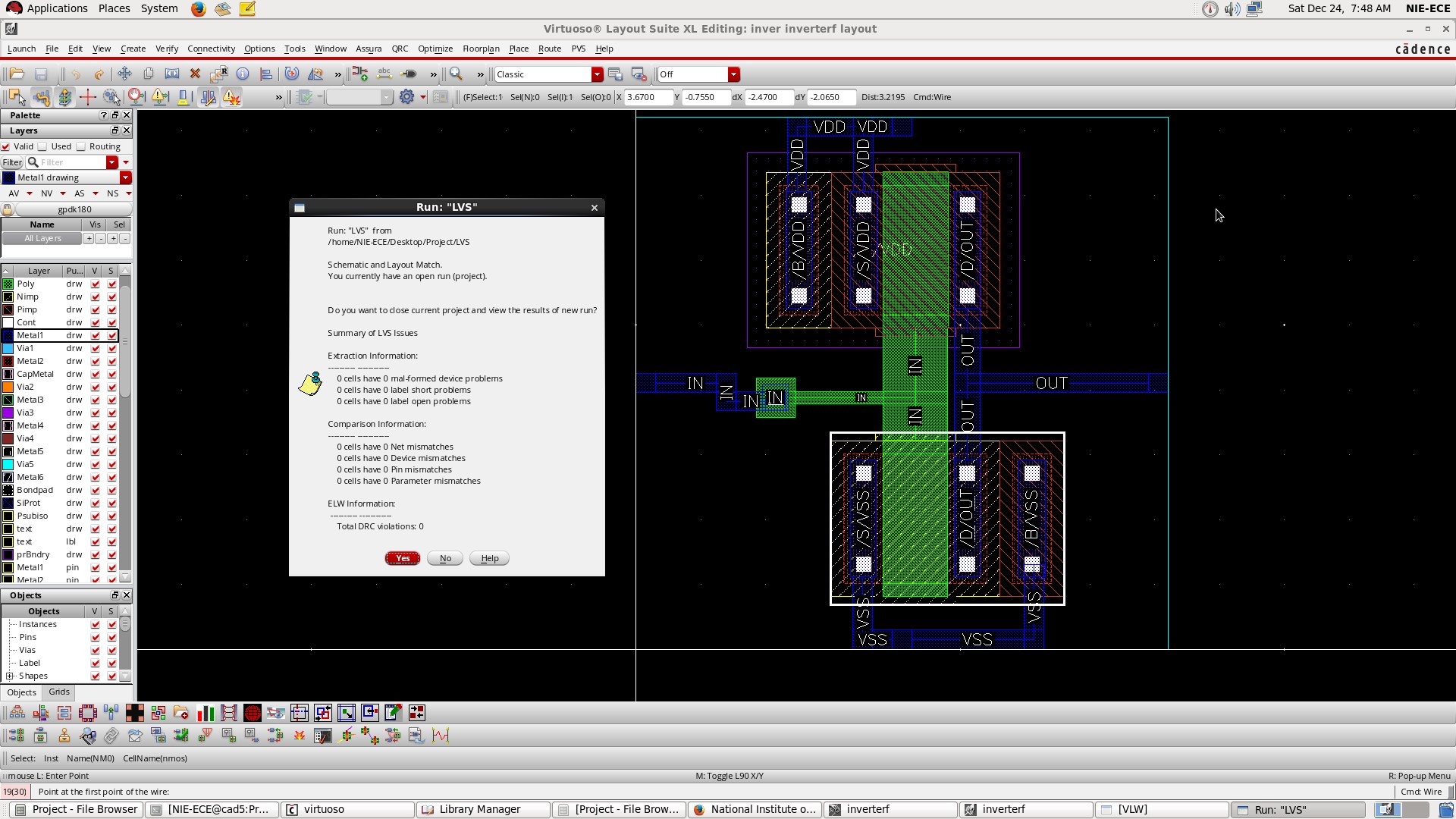


Figure 7: Inverter Layout

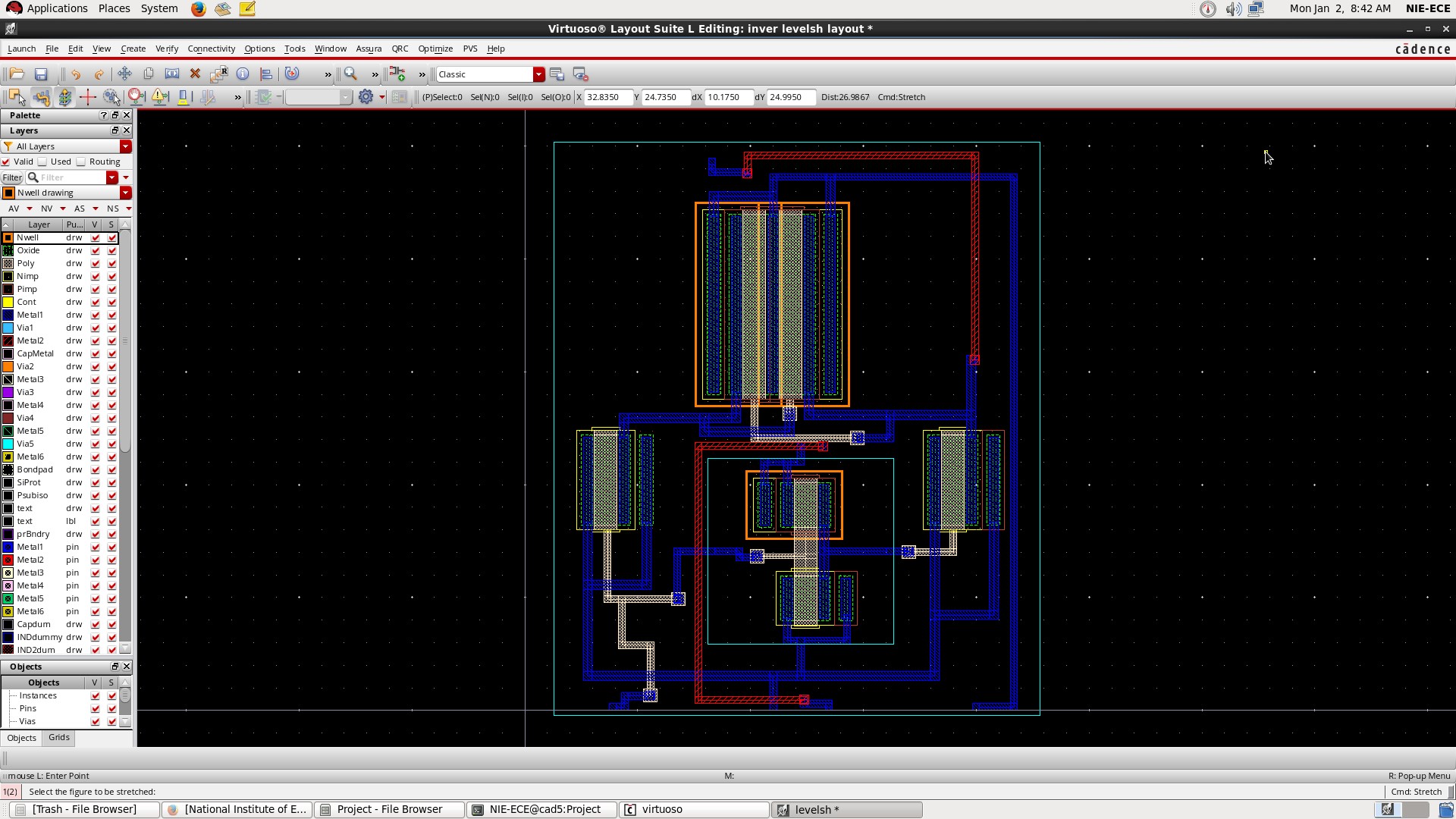


Figure 8: Level Shifter Layout

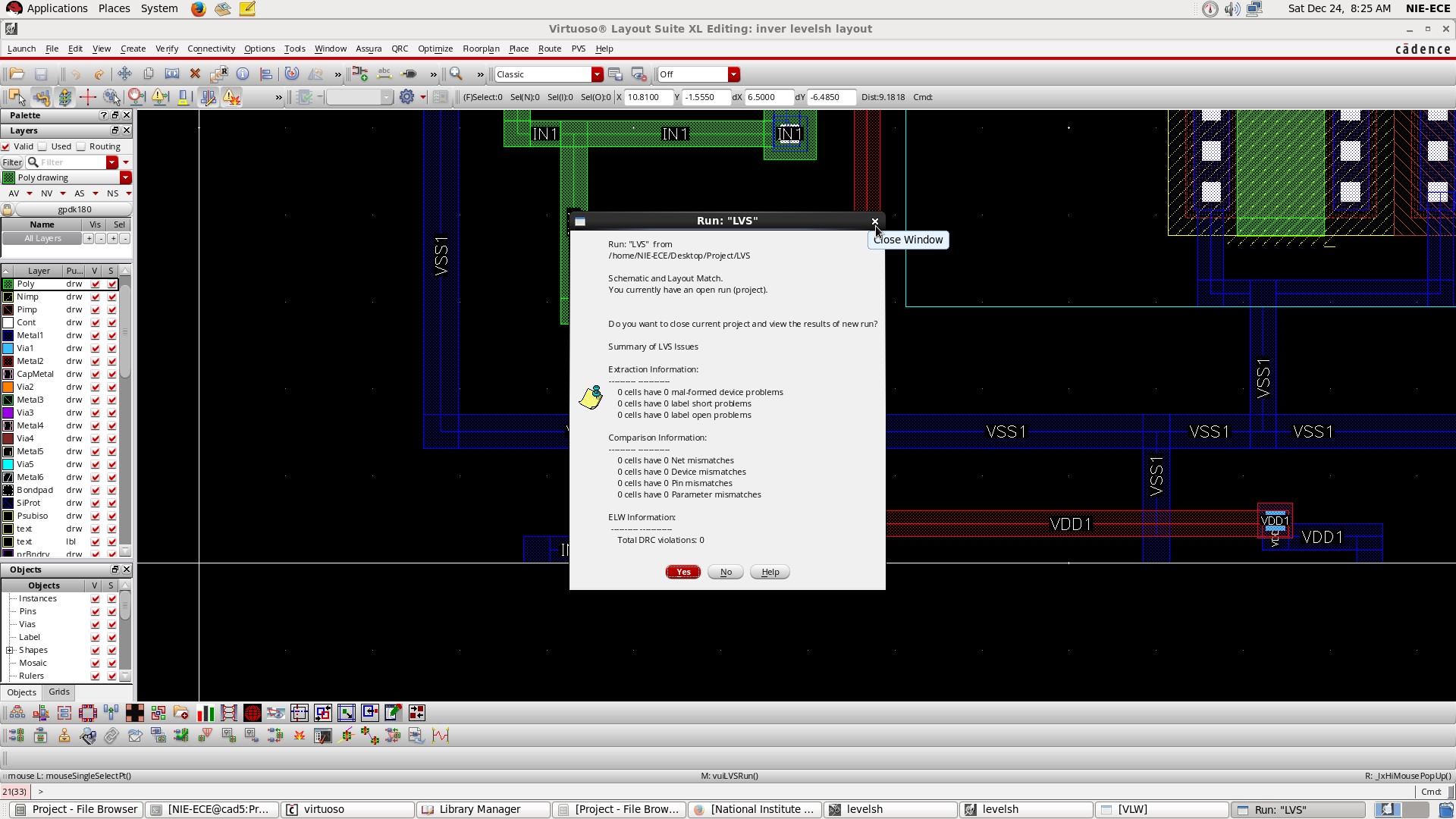


Figure 9: Level Shifter Layout LVS Check

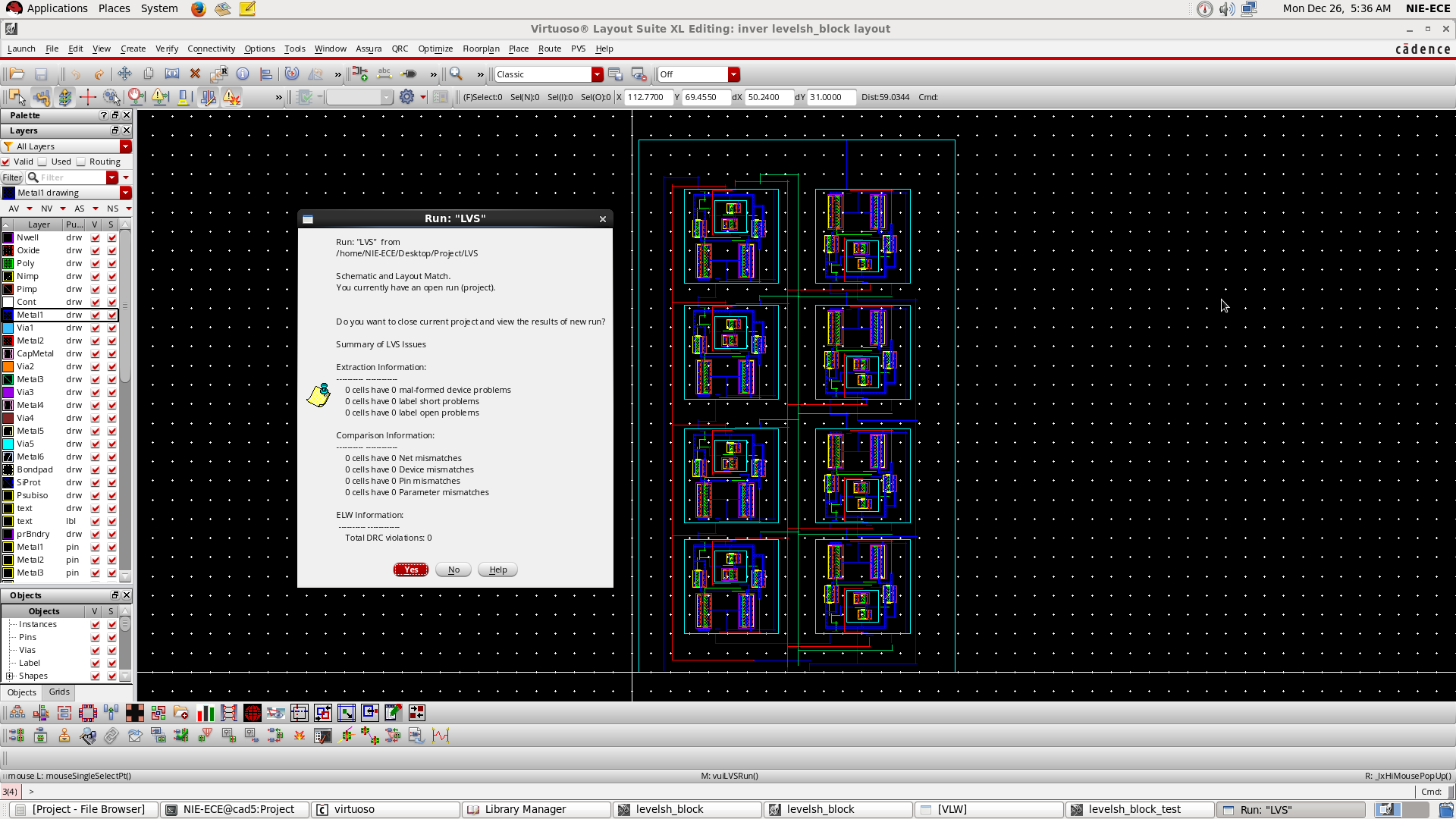


Figure 10: 8-bit Level Shifter Layout

## Simulation

Case [1] : Input is given a pulse of lowest value of 0V and Highest value of 1V. When power supply , VDD2 is 1.2 V , when input pulse goes from 0 to 1V that is to high state

, output goes high to VDD2 value. When input pulse goes low , output pulse also goes low. Here output is level shifted to 1.2V

levels levels\_test schematic 05:15:56 Mon Jan 2 2023

**Transient Response Mon Jan 2 05:15:00 2023**

Name Vis

 /net3

**1.1**

**1.0**

**0.9**

**0.8**

**0.7**

**0.5**

**V (V)**

**0.4**

**0.3**

**0.2**

**0.1**

**0.0**

 /vout

**-0.1**

**1.3**

**1.2**

**1.1**

**1.0**

**0.9**

**0.8**

**0.6**

**V (V)**

**0.5**

**0.4**

**0.3**

**0.2**

**0.1**

**0.0**

**-0.1**

**0.0 4.0 8.0 12.0 16.0 20.0 24.0 28.0 32.0 36.0 40.0**

**time (ms)**

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Figure 11: Transient Response

Case [2] :When power supply VDD2 is increased upto 18V , output pulse also gets pulled upto 18V and hence it gets level shifted .

levels levels\_test schematic 05:14:33 Mon Jan 2 2023

**Transient Response Mon Jan 2 05:12:06 2023**

Name Vis

 /net3

 /vout

**1.1**

**1.0**

**0.9**

**0.7**

**0.6**

**V (V)**

**0.5**

**0.4**

**0.3**

**0.2**

**0.1**

**0.0**

**-0.1**

**19**

**17**

**15**

**13**

**11**

**9.0**

**V (V)**

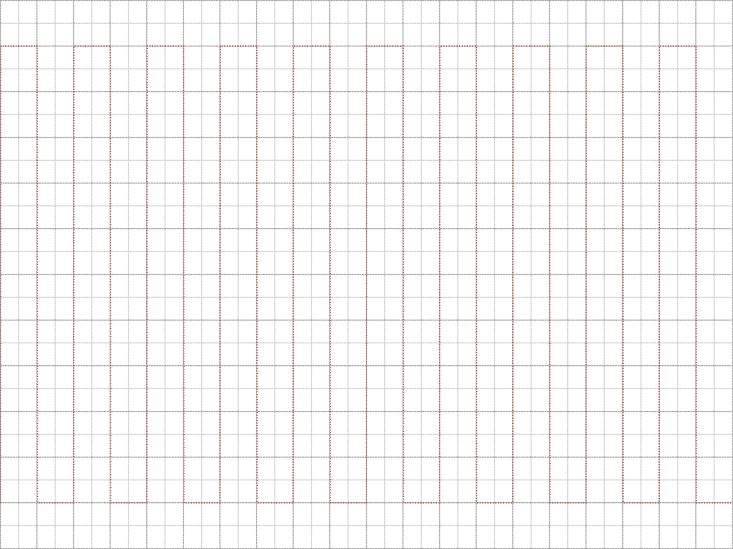
**7.0**

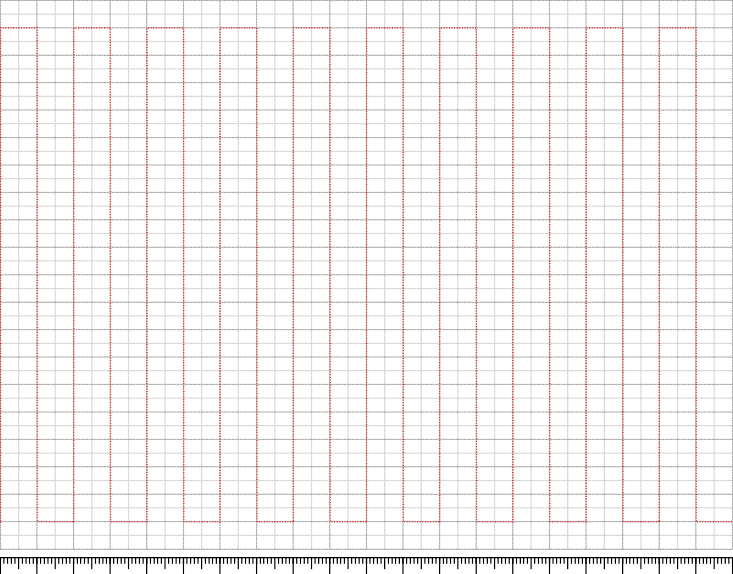
**5.0**

**3.0**

**1.0**

**-1.0**

**0.0 4.0 8.0 12.0 16.0 20.0 24.0 28.0 32.0 36.0 40.0**

**time (ms)**

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Figure 12: Transient Response

inver level\_test schematic 07:27:18 Sat Dec 24 2022

**DC Response Sat Dec 24 07:26:49 2022**

Name Vis



/net3



/OUT2

**1.3**

**1.2**

**1.1**

**1.0**

**0.8**

**0.7**

**0.6**

**V (V)**

**0.5**

**0.4**

**0.3**

**0.2**

**0.1**

**0.0**

**-0.1**

**0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2**

**dc (V)**

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Figure 13: DC Response

## Conclusion and Inference

In this work the design, simulation, and layout, of level shifter covering a wide range of input and output operating voltages were presented.

The level shifter supports a wide range of voltage conversion and it reaches high- speed performance. The post layout simulation result shows that it is able to convert the 1 V input signal into 1.2V to 18V output voltage signal.

The designed Level Shifter is suitable for memory circuits of low power applications and can be widely used in different electronic devices to form efficient SoCs.

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